AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A synchronizer for mapping an electrical digital signal of arbitrary transmission rate for transport over a network characterized by a range of allowable transmission rates, said synchronizer comprising:

a) an input for receiving the electrical digital signal;

b) a data recovery unit coupled to said input, said data recovery unit operative to recover from the electrical digital signal a stream of data bits and a first data clock signal indicative of the arbitrary transmission rate;

c) a clock generator unit coupled to said data recovery unit for receiving the first data clock signal, said clock generator unit being operative to ~~process the first data clock signal for generating~~ generate a second data clock signal by applying a frequency multiplication to the first data clock signal, whereby the second data clock signal is indicative of a line transmission rate that falls within the range of allowable transmission rates for the ~~optical~~ network;

d) a mapping unit in communication with said clock generator unit for receiving the second data clock signal, said mapping unit being operative for mapping the stream of data bits into at least one frame at a line transmission rate indicated by the second data clock signal;

e) an output for releasing the at least one frame from said synchronizer for transmission over the network.

2. (original) A synchronizer as defined in claim 1, wherein the network is an optical network.

3. (original) A synchronizer as defined in claim 2, wherein the optical network is an asynchronous optical network.

4. (original) A synchronizer as defined in claim 1, wherein the network is an electrical network.

5. (original) A synchronizer as defined in claim 4, wherein the electrical network is an asynchronous electrical network.

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6. (original) A synchronizer as defined in claim 1, wherein the at least one frame is characterized by valid timeslots and invalid timeslots, said mapping unit being operative to distribute the bits of the stream of data bits in the valid time slots and providing stuff bits in the invalid time slots.

7. (original) A synchronizer as defined in claim 6, wherein said clock generator unit includes a multiplier.

8. (original) A synchronizer as defined in claim 7, wherein said clock generator includes one input to receive the first data clock signal and another input to receive a control signal, said multiplier being operative to multiply a frequency of the first data clock signal by a value indicated by the control signal to generate the second data clock signal.

9. (currently amended) A desynchronizer for reverse mapping a data signal received from a network, the data signal being characterized by a line transmission rate and including data indicative of an arbitrary transmission rate, said desynchronizer comprising:

a) an input for receiving the data signal from the network;

b) a clock recovery unit coupled to said input, said clock recovery unit operative to recover from the data signal a data clock signal indicative of the line transmission rate;

c) a reverse mapping unit operative to extract from the data signal:

i) a stream of data bits on a basis of the line transmission rate; and

ii) the data indicative of an arbitrary transmission rate;

d) a data transmitter unit coupled to said reverse mapping unit for transmitting the extracted stream of data bits at the ~~a selected~~ arbitrary transmission rate;

e) an output for releasing an electrical signal containing the extracted stream of data bits at the ~~selected~~ arbitrary transmission rate.

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10. (currently amended) A method for transmitting an electrical digital signal of arbitrary transmission rate over a network characterized by a range of allowable transmission rates, comprising:

a) recovering from the electrical digital signal a stream of data bits and a first data clock signal indicative of the arbitrary transmission rate;

b) ~~processing the first data clock signal for~~ generating a second data clock signal by applying a frequency multiplication to the first data clock signal, whereby the second data clock signal is indicative of a line transmission rate that falls within the range of allowable transmission rates for the network;

c) mapping the stream of data bits into at least one frame at a line transmission rate indicated by the second data clock signal;

d) releasing an output signal containing the at least one frame.

11. (original) A method as defined in claim 10 wherein the network is an

optical network.

12. (original) A method as defined in claim 11, wherein the optical network is an asynchronous optical network.

13. (currently amended) A method as defined in claim ~~12~~ 10 wherein the network is an electrical network.

14. (original) A method as defined in claim 13, wherein the electrical network is an asynchronous electrical network.

15. (original) A method as defined in claim 10, wherein the at least one frame is characterized by valid timeslots and invalid timeslots, the step of mapping the stream of data bits into at least one frame including distributing the bits of the stream of data bits in the valid time slots and providing stuff bits in the invalid time slots.

16. (currently amended) A synchronizer for mapping an electrical digital signal of arbitrary transmission rate for transport over a network characterized by a range of allowable transmission rates, said synchronizer comprising:

a) input means for receiving the electrical digital signal;

b) data recovery means coupled to said input means, said data recovery means operative to recover from the electrical digital signal a stream of data bits and a first data clock signal indicative of the arbitrary transmission rate;

c) clock generator means coupled to said data recovery means for receiving the first data clock signal, said clock generator means being operative to ~~process the first data clock signal for generating~~ generate a second data clock signal by applying a frequency multiplication to the first data clock signal, whereby the second data clock signal is indicative of a line transmission rate that falls within

the range of allowable transmission rates for the ~~optical~~ network;

d) mapping means in communication with said clock generator means for receiving said second data clock signal, said mapping means being operative for mapping the stream of data bits into at least one frame at a line transmission rate indicated by the second data clock signal;

e) output means for releasing the at least one frame from said synchronizer for transmission over the network.